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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,682	12/07/2005	Martin Wany	Q96159	6166

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
WILLIAMS, DON J	

ART UNIT	PAPER NUMBER
2878	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,682	WANY ET AL.	
	Examiner	Art Unit	
	Don Williams	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 April 2005 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 4/24/07, 4/27/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosier et al (6,847,400) in view of Krymski (7,050,094).

As to claim 1, Hosier et al disclose a (photodiode, 10) which can be connected to (reset voltage, VR1) to define a first potential (V_{reset}, V_{reset1}) via (transistor, T1) to define a first transistor or a first diode (photodiode, 10), the (photodiode, 10) can furthermore be connected to the input of (output amplifier, 16) to define a readout amplifier via (Sampling and Hold transistor, SH) to define a second transistor, (transistor, R2) to define a third transistor via which the input of the readout amplifier (output amplifier, 16) can be connected to (reset voltage, V_{R2}) to define a second potential (V_{reset}, V_{reset2}) furthermore being arranged between the second transistor (Sampling and Hold transistor, SH) and the input of the readout amplifier (output amplifier, 16), and in that there are (Holding Capacitor, C_H; node capacitor, C_P) to define means which allow temporary storage of the integrated signal value (integrated light signal, V_{sig}) until the readout time (integration time periods, A-D), (fig. 1 column 3, lines 38-67, fig. 2, column 4, lines 20-54), (column 5, lines 33-37). Hosier et al fail to explicitly disclose a large

dynamic range. Hosier et al and Krymski are related optoelectronic imaging devices. Krymski disclose a wide dynamic range operation is used to write a signal in a freeze-frame pixel into memory twice, first after short integration and then after long integration, (Abstract, fig. 1, column 2, lines 1-15, lines 36-45). It would have been obvious for one of ordinary skill in the art to modify Hosier et al to include the wide dynamic range operation as taught by Krymski to improve the intra-scene dynamic range of images to be extended by combining the image taken with a short exposure time with the image taken with a long exposure time resulting in optimal utilization of the device.

As to claim 2, Hosier et al disclose a first transistor (T1), a first potential (reset voltage, V_{R1}), and a second potential (reset voltage, V_{R2}), (fig. 1, column 3, lines 45-67). Hosier et al fail to explicitly disclose that the first and second potentials are at the same voltage level. It is well known in the art to have reset potentials at the same voltage level in order to obtain consistent signal processing to improve signal to noise ratio. It would have been obvious for one of ordinary skill in the art to modify Hosier et al to set the reset potentials at the same voltage level in order to acquire consistent integration of signal processing resulting in a wide dynamic range of signal processing and improved signal to noise ratio throughout the device.

As to claim 3, Hosier et al disclose additional conversion node capacitor (capacitance, C_P) to ground potential is arranged between the second transistor (Sampling and Hold transistor, SH) and the input of the readout amplifier (output amplifier, 16), (fig. 1, column 3, lines 31-33, lines 60-67).

As to claim 4, Hosier et al disclose the readout amplifier (output amplifier, 16), an (output line, 18), and that the image signal charges (integrated light signal, V_{sig}) are amplified and transferred to a common output line or bus through successively actuated multiplexing transistors which constitutes that which is claimed (column 1, lines 33-35, fig. 1, column 3, lines 26-35). Hosier et al fail to explicitly disclose row selection transistor. It is well known in the art to use row selection transistors in order to transfer output signals to imaging processing circuitry. It would have been obvious for one of ordinary skill in the art to modify Hosier et al to include row selection transistors in order to output the amplified signal to image processing circuitry to improve the sensitivity to obtain good signal to noise ratio throughout the device resulting in acquiring a large dynamic range.

As to claim 5, Hosier et al disclose transistors, (T1, FZ, T2, R1, SH, R2), (fig. 1, column 3, lines 50-65). Hosier et al fail to explicitly disclose that the transistors are designed as MOS transistors. It is well known in the art to use MOS transistors to reset and transfer signals. It would have been obvious for one of ordinary skill in the art to use the transistors as taught by Hosier et al as MOS transistors in order to improve the integration time of resetting and transferring signals resulting in a reduction of noise level to acquire high quality imaging.

As to claim 6, Hosier et al disclose the gate voltage (V_{R2}) of the second transistor (Sampling and Hold, SH) is controlled so that the current (integrated light signal, V_{sig}) generated by the (photodiode, 10) discharges only a capacitor (C_H, C_P) at the input of the readout amplifier (output amplifier, 16) in a first phase of the integration time

(integration time periods, A-D), and in that the gate voltage (V_{R1}) of the first transistor (T1), or respectively the first potential (Vreset1) (reset voltage, V_{R1}) when there is a first diode (photodiode, 10), is in this case controlled so that some or all of the current (integrated light signal, V_{sig}) generated by the (photodiode, 10) is compensated for by the channel of the first transistor (T1) or respectively by the first diode (photodiode, 10) in a last phase of the integration time (integration time periods, A-D), (fig. 1, column 3, lines 25-67, fig. 2, column 4, lines 15-54, (column 5, lines 33-37).

As to claim 7, Hosier et al disclose the gate voltage (V_{R1}) of the first transistor (T1) is lower than the gate voltage (V_{R2}) of the second transistor (Sampling and Hold, SH) and in that the gate voltage (V_{R1}) of the first transistor (T1) is higher than the saturation signal (resulting signal, $V_{R2}+V_{sig}$) of the readout buffer (readout amplifier, 16) by a threshold voltage (reference voltage), or respectively in the case of a first diode (photodiode, 10), the diode anode voltage (integrated light signal, V_{sig}) of the first diode (photodiode, 10) is adjusted (reset) by the first potential (V_{reset1}) (reset voltage, V_{R1}) so that this anode voltage (integrated light signal, V_{sig}) minus the diode threshold voltage (reference voltage) is lower than the gate voltage (VR1, VR2) minus the threshold voltage (reference voltage) of the second transistor (Sampling and Hold transistor, SH) and in that the diode anode voltage (integrated light signal, V_{sig}) of the first diode (photodiode, 10) is higher than the saturation signal (VR2+Vsig) of the readout buffer (output amplifier, 16) by a diode threshold voltage (reference voltage), (fig. 1, column 3, lines 33-67, fig. 2, column 4, lines 15-54, column 5, lines 33-38).

As to claim 8, Hosier et al disclose two gate voltages (VR1, VR2), and threshold voltages (reference voltage) and subtraction circuit, (fig. 1, column 3, lines 50-67, column 4, lines 15-54, column 5, lines 23-30). Hosier et al fail to explicitly disclose the tolerance of the reference values plus the tolerance of the voltage values and that the difference is 100mv. It is well known in the art to use subtraction circuit to extrapolate undesired signals while maintaining desired light signals. It would have been obvious for one of ordinary skill in the art to use the subtraction circuit as taught by Hosier et al to manipulate the reference and voltage signals in order to acquire a value greater than 100 mv.

As to claim 9, Hosier et al disclose the gate voltage (V_{R1}) of the first transistor (T1) and the gate voltage (V_{R2}) of the second transistor (Sampling and Hold, SH) can be varied (reset) during the integration time (integration time periods, A-D), (fig. 1, column 3, lines 50-67, fig. 2, column 4, lines 15-54).

As to claim 10, Hosier et al disclose the gate voltage (V_{R1}) of the (first transistor, T1), or respectively the first potential (V_{reset1}) (reset voltage, V_{R1}) in the case of a first diode (photodiode, 10), and the gate voltage (V_{R2}) of the second transistor (Sampling and Hold transistor, SH), is respectively adjusted (reset) or controlled so that charge carriers (integrated light signal, V_{sig}) accumulated by the (photodiode, 10) discharge only a conversion node capacitor (C_M, C_R, C_P, C_L) in a first phase of the integration time (integration time periods, A-D), in that charge carriers (integrated light signal, V_{sig}) accumulated by the (photodiode, 10) discharge (reset) both a photodiode capacitor (C_M) and conversion node capacitors (C_M, C_R, C_P, C_L) in a second phase after an equal

potential (reset voltages, V_{R1}, V_{R2}) has been reached at the output of the (photodiode, 10) and at the input of the readout amplifier (output amplifier, 16), and in that after the output (integrated light signal, V_{sig}) of the (photodiode, 10) has fallen below the threshold value (reference voltage) of the first transistor (T1) or respectively the diode threshold value (reference voltage) of the first diode (photodiode, 10), charge carriers (integrated light signal, V_{sig}) accumulated by the (photodiode, 10) are made available via the first transistor (T1) or respectively via the first diode (photodiode, 10) in a third phase, and the second transistor (Sampling and Hold transistor, SH) is opened after the integration time (integration time periods, A-D), has elapsed so that the signal (integration light signal, V_{sig}) is held at the conversion capacitor (C_P) until the readout time (integration time periods, A-D) and in that the first transistor (T1) or respectively the first diode (photodiode, 10) is adjusted (reset) during this holding time so that the photodiode capacitor (C_M) is not fully discharged (reset), (fig. 1, column 3, lines 25-65, fig. 2, column 4, lines 15-54).

As to claim 11, Hosier et al disclose that the gate voltage (V_{R2}) of the second transistor (Sampling and Hold transistor, SH) is adjusted (reset) during the reset phase and during the integration phase (integration time periods, A-D) so that the gate voltage (V_{R2}) minus the threshold voltage (reference voltage) is lower than the reset voltage (voltage reset, VR1, VR2) which is set at the input of the readout amplifier (output amplifier, 16) and in that the gate voltage is higher than the saturation voltage (resulting signal, VR2+Vsig) of the readout buffer (output line, 18) by a threshold voltage (reference voltage), (fig. 1, column 3, lines 60-67, fig. 2, column 4, lines 15-54).

As to claim 12, Hosier et al disclose the gate voltage (V_{R2}) of the second transistor (Sampling and Hold transistor, SH) is varied (reset) during the integration phase (integration time periods, A-D), although it always remain greater than the gate voltage (V_{R1}) of the first transistor (T1), and in that the gate voltage (V_{R1}) of the first transistor (T1) is preferably reduced successively during the integration phase (integration time periods, A-D)), (column 1, lines 33-36, fig. 1, column 3, lines 60-67, fig. 2, lines 15-54).

As to claim 13, Hosier et al disclose the gate voltage (V_{R1}) of the first transistor (T1) is constant or successively reduced during the integration time (integration time periods, A-D), (column 1, lines 33-36, fig. 1, column 4, lines 15-54).

As to claim 14, Hosier et al disclose that the gate voltage (V_{R2}) of the second transistor (Sampling and Hold transistor, SH) is switched (reset) once so that it is equal to the bulk potential ($V_{R2}+V_{sig}$) of the (Sampling and Hold transistor, SH) and is switched (reset) back again to it original value (V_{R2}), (fig. 1, column 3, lines 60-67, fig. 2, column 4, lines 15-54).

As to claim 15, Hosier et al disclose linear arrays of photosites: charge coupled devices or CCDs, or CMOS to define one-two dimensional array of optoelectronic sensors, (column 1, lines 38-45).

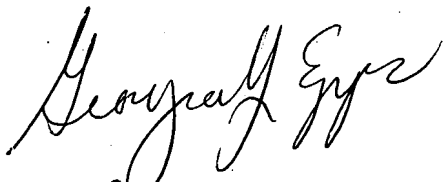
As to claim 16, Hosier et al disclose operating linear arrays of photosites: charge coupled devices or CCDs, or CMOS, (column 1, lines 38-45).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don Williams whose telephone number is 571-272-8538. The examiner can normally be reached on 8:30a.m. to 5:30a.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on 571-272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Georgia Epps
Supervisory Patent Examiner
Technology Center 2800